Amendments to the Specification

Please add the following replacement paragraphs for paragraphs [0001], [0002], [0030], [0031], and [0033]:

**[0001]** This application is related to co-pending U.S. patent application 10/623,390, Attorney Docket No. ONS00502, entitled "DC/DC CONVERTER WITH DEPLETION MODE COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR SWITCHING DEVICE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.

**[0002]** This application is further related to co-pending U.S. patent application 10/623,392, Attorney Docket No. ONS00505, entitled "METHOD OF MAKING A VERTICAL COMPOUND SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE", by Peyman Hadizad, assigned to the same assignee, Semiconductor Components Industries, LLC, filed concurrently herewith, and which is incorporated by reference for all purposes.

**[0030]** Openings are then formed in dielectric layer 63 to provide contacts to source regions 26. Additionally, portions of trench-fill layer 66 and passivation layer 63 are removed to expose portions of a gate connecting region 79 (shown in FIG. 2). A first metal or contact layer is formed over upper surface 19, and patterned to provide a source contact 84 and a gate contact 86 (shown in FIG. 2). Source contact layer 84 and gate contact layer 86 preferably comprise NiGeAu, NiGeW, or ~~other~~ another suitable metal. A second contact layer or metal layer 87 is formed over source contact 84 and gate contact 86. Second metal layer 87 preferably comprises nickel or gold, and is formed using electroplating or electroless plating techniques. Body of

semiconductor material 13 is thinned using a backgrind step, and a back metal or drain contact layer 88 is deposited on lower surface 21. Drain contact layer 88 comprises NiGeAu, or another suitable metal.

**[0031]** FIG. 2 shows an enlarged partial top plan view of a preferred gate contact structure 71, which includes doped connecting region 79. Doped gate connecting region 79 ties or couples together a plurality of doped gate regions 59 in a single contact region. For ease of understanding, structure 11 shown in FIG. 1 is taken along reference line 1-1 of FIG. 2. Phantom line 89 represents an alternative placement for gate contact layer 86. Doped termination region 159 and termination contact layer 186 ~~is~~ are part of a preferred termination structure 91, which is described next in FIG. 3.

**[0033]** By using multiple trench structure 28 according to the present invention, gate region 59 is placed deeper into channel regions 61 and is more separated from source regions 26 thereby improving gate blocking characteristics. Also, by using a doped gate region, the blocking characteristics are further improved compared to conventional Schottky gate designs. Also, because structure 11 comprises a compound semiconductor material, structure 11 has a reduced gate charge, ~~reduce~~ reduced gate resistance, and enhanced switching speeds compared to silicon based devices.